IN THE CLAIMS

Claims 1-10 (Canceled).

11 (Original). A memory comprising:

an insulator over a substrate, said insulator including a pore having an electrode over the substrate and a phase change material over the electrode, wherein the phase change material fills less of the pore than the electrode.

12 (Original). The memory of claim 11 wherein said phase change material fills less than 25 percent of the pore.

13 (Original). The memory of claim 11 wherein said phase change material fills about 10 percent or less of the pore.

14 (Original). The memory of claim 11 wherein said phase change material is entirely contained within the pore.

15 (Original). The memory of claim 11 wherein said phase change material is a chalcogenide.

16 (Original). The memory of claim 11, said electrode to act as a heater to heat said phase change material.

17 (Original). The memory of claim 11 wherein the phase change material is substantially co-planar with the upper surface of said insulator.

18 (Original). The memory of claim 11 including a select device coupled to said electrode.

19 (Original). The memory of claim 11 including a conductive line formed over said insulator and said phase change material.

20 (Original). The memory of claim 19 wherein said phase change material is in contact with said conductive line.

21 (Original). The memory of claim 19 wherein said conductive line and the upper surface of said electrode are substantially parallel.

22 (Original). A system comprising:

a processor-based device;

a wireless interface coupled to said processor-based device; and

a semiconductor memory coupled to said device, said memory including an insulator over a substrate, said insulator including a pore having an electrode over the substrate and a phase change material over the electrode wherein the phase change material fills less of the pore than the electrode.

23 (Original). The system of claim 22 wherein said phase change material fills less than 25 percent of the pore.

24 (Original). The system of claim 22 wherein said phase change material fills about 10 percent or less of the pore.

25 (Original). A memory comprising:

an insulator over a substrate, said insulator including a pore having an electrode over the substrate and a phase change material over the electrode, wherein the phase change material is less than 25 percent of the height of the pore.

26 (Original). The memory of claim 25 wherein said phase change material is about 10 percent or less of the height of the pore.

27 (Original). The memory of claim 26 wherein said phase change material fills less of the pore than the electrode.

28 (Original). The memory of claim 27 wherein said phase change material fills about 10 percent or less of the pore.

29 (Original). The memory of claim 25 wherein said phase change material is entirely contained within the pore.

30 (Original). The memory of claim 29 including a conductive line over said phase change material wherein said conductive line and the upper surface of said electrode are substantially parallel.

31 (Original). An apparatus comprising:

a damascene structure, wherein the damascene structure includes a first electrode over a substrate and a phase change material over the first electrode; and

a second electrode over the damascene structure.

32 (Original). The apparatus of claim 31 wherein the damascene structure further comprises an insulator having a pore over the substrate, wherein the first electrode and the phase change material are formed in the pore.